What is claimed is:

1. A crosstalk cancellation circuit for suppressing crosstalk noise of interconnections in an integrated circuit, comprising:

N (N is an even number of 2 or more) number of first inverters;

a first interconnection for connecting the N number of first inverters in series;

N number of second inverters; and

a second interconnection for connecting said N number of second inverters in series, and

wherein said first and second interconnections are arranged adjacent in parallel or substantially parallel to each other,

wherein at least one first inverters among said N number of first inverters is arranged at a location where crosstalk noise due to a parasitic capacity between said first and second interconnections is canceled out or substantially canceled out on said second interconnection, and

wherein at least one second inverter among said N number of second inverters is arranged at a location where crosstalk noise due to a parasitic capacity between said first and second interconnections is canceled out or substantially canceled out on said

first interconnection.

2. A crosstalk cancellation circuit as set forth in claim 1, wherein

said N number of first inverters are arranged in the approximately same interval in said first interconnection, and

said N number of second inverters are arranged in said second interconnection at the middle positions where distances from the adjacent first inverters are equal.

3. A crosstalk cancellation circuit as set forth in claim 1, wherein,

in each of said N number of first inverters, a time when an input signal voltage of the related first inverter changes and a time when an output signal voltage changes overlap, and

in each of said N number of second inverters, a time when the input signal voltage of the related second inverter changes and a time when the output signal voltage changes overlap.

4. A crosstalk cancellation circuit as set forth in claim 1, wherein said N number of first and second inverters and said first and second interconnections comprise buses in said integrated circuit.

5. A crosstalk cancellation circuit as set forth in claim 1, wherein said N number of first and second inverters are inverters having the same configuration.

6. An interconnection module in an integrated circuit, comprising:

M (M is a natural number) number of inverters;

input lines of said M number of inverters;

output lines of said M number inverters; and

L number of signal lines, and

wherein said input lines, said output lines, and said signal lines are parallel or substantially parallel to each other, and wherein said inverters, input lines, and output lines of the related inverters and said signal lines are alternately arranged (note, where M=1, L=M or L=M+1 and where M≥2, L=M, L=M+1, or L=M-1).

7. An interconnection module as set forth in claim 6, wherein

M is an integer of 2 or more, and

said M number of inverters are arranged so as to be parallel in a direction vertical or substantially vertical to the direction of said signal lines.

8. An interconnection module as set forth in claim 6, wherein said integrated circuit is configured as

a semiconductor integrated circuit manufactured by a process rule of less than 0.25 micrometer.

9. A method of interconnection of an automatic interconnection apparatus for laying out interconnections in an integrated circuit, comprising the steps of:

a first step of arranging a plurality of interconnections parallel or substantially parallel; and

a second step of inserting the same number of inverters at said plurality of interconnections, and

wherein said second step having a third step of inserting each inverter at a location where crosstalk noise due to a parasitic capacity of the adjoining interconnections is canceled out or substantially canceled out on the related adjoining interconnections.

10. A method of interconnection of an automatic interconnection apparatus as set forth in claim 9, wherein, in said third step, said inverters are inserted at alternate locations with respect to the interconnections adjoining each other among said plurality of interconnections.

11. A method of interconnection of an automatic interconnection apparatus as set forth in claim 9, wherein, in said third step, each inverter is inserted at one interconnection between interconnections adjoining each other at a location where the distance from the

inverter of the other interconnection becomes the maximum or in the vicinity of that location.

12. A method of interconnection of an automatic interconnection apparatus as set forth in claim 9, wherein a time when an input signal voltage changes and a time when an output signal voltage changes overlap.

13. A method of interconnection of an automatic interconnection apparatus as set forth in claim 9, wherein said interconnections are interconnections of buses.

14. A method of interconnection of an automatic interconnection apparatus as set forth in claim 9, wherein said integrated circuit is configured as a semiconductor integrated circuit manufactured by a process rule of less than 0.25 micrometer.

15. A method of interconnection of an automatic interconnection apparatus as set forth in claim 9, wherein the inverters inserted at said plurality of interconnections are inverters having the same configuration.

16. An integrated circuit comprising

a crosstalk cancellation circuit for suppressing crosstalk noise of interconnections in an integrated circuit, and

wherein said crosstalk cancellation circuit

comprises

N (N is an even number of 2 or more) number of first inverters,

a first interconnection for connecting the N number of first inverters in series, N number of second inverters, and

a second interconnection for connecting said N number of second inverters in series, and

Wherein said first and second interconnections are arranged adjacent in parallel or substantially parallel to each other,

wherein at least one first inverters among said N number of first inverters is arranged at a location where crosstalk noise due to a parasitic capacity between said first and second interconnections is canceled out or substantially canceled out on said second interconnection, and

wherein at least one second inverter among said N number of second inverters is arranged at a location where crosstalk noise due to a parasitic capacity between said first and second interconnections is canceled out or substantially canceled out on said first interconnection.